PILLAR CELL FLASH MEMORY TECHNOLOGY

ABSTRACT OF THE DISCLOSURE

An array of a pillar-type nonvolatile memory cells (803) has each memory cell isolated from adjacent memory cells by a trench (810). Each memory cell is formed by a stacking process layers on a substrate: tunnel oxide layer (815), polysilicon floating gate layer (819), ONO or oxide layer (822), polysilicon control gate layer (825). Many aspects of the process are self-aligned. An array of these memory cells will require less segmentation. Furthermore, the memory cell has enhanced programming characteristics because electrons are directed at a normal or nearly normal angle (843) to the floating gate (819).